What is claimed is:

1. A data processor comprising:

a CPU;

an internal memory accessible by said CPU; and

a control circuit capable of responding to a particular access request issued by said CPU to control a block transfer, in which said internal memory is used as one transfer object,

wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request,

the particular instruction has an addressing field, and

when an address specified by the addressing field coincides with an address mapped to said internal memory, the address is set as one of transfer source and transfer destination addresses of the block transfer.

2. The data processor of Claim 1, wherein the other of the transfer source and transfer destination addresses of the block transfer is a physical address corresponding to a logical address held by the addressing field.

3. The data processor of Claim 1, wherein the other of the transfer source and transfer destination addresses of the block transfer is a physical address held by a register.

4. The data processor of Claim 3, wherein said register is mapped to an address space of said CPU.

5. The data processor of Claim 2, further comprising a

bus interface controller connected to said control circuit,

wherein said bus interface controller is capable of performing interface control of the other transfer object.

6. The data processor of Claim 1, further comprising a cache memory,

wherein said cache memory shares a first bus with said CPU, internal memory, and control circuit.

7. The data processor of Claim 6, wherein said internal memory is assigned a cache non-object address for said cache memory.

8. The data processor of Claim 7, further comprising a second bus used exclusively for connecting said control circuit with said internal memory,

wherein said second bus can be utilized for data block transfer in response to the particular access request.

9. The data processor of Claim 8, wherein said control circuit is capable of performing memory control in regard to a cache hit and cache miss with respect to said cache memory.

10. The data processor of Claim 7, wherein the set of instructions for said CPU includes a first cache memory-operating instruction, and

the first cache memory-operating instruction causes an operation of making said cache memory retain data at a cache object address specified by the addressing field.

11. The data processor of Claim 7, wherein the set of

instructions for said CPU includes a second cache memory-operating instruction, and

when a cache hit is detected at a cache object address specified by the addressing field and a cache entry associated with the cache hit is dirty, the second cache memory-operating instruction causes an operation of writing back the cache entry.

12. The data processor of Claim 10, wherein the particular instruction has an operation code identical with that of the first cache memory-operating instruction, and sets the cache non-object address of the addressing field as the destination address.

13. The data processor of Claim 11, wherein the particular instruction has an operation code identical with that of the second cache memory-operating instruction, and sets the cache non-object address of the addressing field as the source address.

14. The data processor of Claim 5, further comprising a data transfer control circuit connected with said bus interface controller.

15. The data processor of Claim 14, further comprising an external interface circuit for connection of an external bus, which is connected with said bus interface controller.

16. A data processor comprising:

a CPU;

a cache memory;

an internal memory accessible by said CPU and set as a

cache non-object for said cache memory;

a control circuit capable of responding to a particular access request issued by said CPU to control a block transfer, in which said internal memory is used as one transfer object; and

a first bus connected with said CPU, cache memory, internal memory, and control circuit,

wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request,

the particular instruction has an addressing field, and

when an address specified by the addressing field coincides with an address mapped to said internal memory, the address is set as one of transfer source and transfer destination addresses of the block transfer.

17. The data processor of Claim 16, further comprising a second bus used exclusively for connecting said control circuit with said internal memory,

wherein said second bus can be utilized for data block transfer in response to the particular access request.

18. The data processor of Claim 17, wherein the set of instructions for said CPU includes a first cache memory-operating instruction, and a second cache memory-operating instruction,

the first cache memory-operating instruction instructs

an operation of making said cache memory retain data at a cache object address specified by the addressing field, and

when a cache hit is detected at a cache object address specified by the addressing field and a cache entry associated with the cache hit is dirty, the second cache memory-operating instruction instructs an operation of writing back the cache entry.

19. The data processor of Claim 18, wherein said particular instruction is one of: a first data transfer instruction which is allocated an operation code identical with that of the first cache memory-operating instruction and which sets the cache non-object address of the addressing field as the destination address; and a second data transfer instruction which is allocated an operation code identical with that of the second cache memory-operating instruction and which sets the cache non-object address of the addressing field as the source address.

20. A data processor comprising:

a CPU;

a bus capable of transmitting an access request issued by the CPU;

an internal memory connected with said bus, capable of operating as a memory in response to the access request issued by said CPU;

a control circuit connected with said bus, capable of responding to a particular access request issued by said CPU

to control a block transfer, in which said internal memory is used as one transfer object; and

a bus interface controller capable of performing interface control of the other transfer object of the block transfer,

wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request, and

the particular instruction has an addressing field for specifying one of transfer source and transfer destination addresses of the block transfer.